

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

WO 02/23716 A2



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

POWER AMPLIFIER CIRCUITRY AND METHOD

FIELD OF THE INVENTION

This invention relates to the field of power amplifiers. More particularly, this
5 invention relates to improved power amplifier circuitry which reduces the peak voltages
to which switching devices of the amplifier are subjected.

BACKGROUND OF THE INVENTION

In some applications utilizing a power amplifier, it is desirable to limit the peak
10 voltage that the switching devices of the power amplifier are subjected to. For example,
in CMOS devices, the transistor breakdown voltage may be only slightly greater than the
supply voltage. Therefore, CMOS devices are not well suited to traditional power
amplifier designs, where switching devices are subjected to voltages at least twice the
supply voltage.

15

Figure 1 is a schematic diagram of a conventional Class E amplifier. As shown, a
transistor M1 is connected between ground and an inductor L1 which is connected to a
voltage source V_{dd} . The gate of the transistor M1 is connected to an input signal V_i . The
connection of the transistor M1 and the inductor L1 forms a node labeled V_d . The
20 switching device M1, as well as other switching devices described may be comprised of
any suitable switching devices, for example, MOSFETs or other transistor types. A
capacitor C1 is connected between V_d and ground. The amplifier includes a

transformation network consisting of inductor L2 and capacitor C2. The capacitor C2 is connected to a load R_L at output node V_o .

Figure 2 is a timing diagram illustrating the input signal V_i and the resulting voltage at V_d . As shown, the input signal V_i is a square wave signal switching between ground and V_{dd} . When the input signal V_i is high (V_{dd}), the transistor M1 is turned on, holding V_d to ground. When the input signal V_i transitions to low, transistor M1 turns off and the voltage at V_d rises above V_{dd} . During this time, the transistor M1 must sustain this high drain-to-source voltage. After peaking, the voltage at V_d decreases until it reaches ground. In a typical prior art Class E design, this peak voltage is approximately $3.6 V_{dd}$. Although the peak voltage can be reduced slightly, it can not be decreased below about $2.5 V_{dd}$ since the average voltage at V_d must equal V_{dd} . Designs such as that shown in Figure 1 are not well suited to certain device technologies, such as CMOS, where transistor breakdown voltages are only slightly higher than the supply voltage.

15

It can therefore be seen that there is a need for amplifier designs where the peak voltages applied to the transistors of the amplifier are reduced so that they are below the transistor breakdown voltages of the devices being used to implement the design.

20 Another problem relating to amplifiers relates to the use of differential circuits. It is difficult to perform differential-to-single-ended conversion when a single ended load is

required with high efficiency. Therefore, there is a need for improved differential-to-single-ended conversion designs.

SUMMARY OF THE INVENTION

5 A power amplifier of the invention includes a first switching device connected between a first supply voltage and a first output node, a second switching device connected between a second supply voltage and a second output node, and an inductance coupled between the first and second output nodes.

10 Another embodiment of the invention provides a method of reducing the peak output voltage in an amplifier including the steps of providing an inductor having first and second terminals, providing a first switching device connected between the first terminal of the inductor and a first supply voltage, providing a second switching device connected between the second terminal of the inductor and a second supply voltage,
15 applying a voltage between the first and second terminals of the inductor during a first portion of a clock cycle by turning on the first and second switching devices, and turning off the first and second switching devices during a second portion of the clock cycle.

 Another embodiment of the invention provides a differential power amplifier
20 including a first amplifier having a first switching device connected between a first supply voltage and a first output node, a second switching device connected between a second supply voltage and a second output node, and an inductance coupled between the

first and second output nodes, a second amplifier having a third switching device connected between a third supply voltage and a third output node, a fourth switching device connected between a fourth supply voltage and a fourth output node, and an inductance coupled between the third and fourth output nodes, and wherein the first and
5 second amplifiers are coupled together to drive a load.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

10 BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

15 Figure 1 is a schematic diagram of a prior art Class E amplifier.

Figure 2 is a timing diagram illustrating the voltage at V_D relative to the input signal V_I for the prior art Class E amplifier shown in Figure 1.

20 Figure 3 is a block diagram illustrating an example of an environment in which a power amplifier of the present invention may be used.

Figure 4 is a schematic diagram of one embodiment of a power amplifier of the present invention.

Figure 5 is a timing diagram illustrating the voltages present in the amplifier
5 shown in Figure 4, relative to the input signals.

Figure 6 is a schematic diagram of an embodiment of a power amplifier of the present invention with a load connected differentially.

10 Figure 7 is a schematic diagram of an embodiment of a power amplifier of the present invention connected to a single-ended load.

Figure 8 is a schematic diagram of an embodiment of a power amplifier of the present invention connected differentially.

15

Figure 9 is a timing diagram illustrating the voltages present in the amplifier shown in Figure 8.

Figure 10 is a schematic diagram of an embodiment of a power amplifier of the
20 present invention.

Figure 11 is a schematic diagram of another embodiment of a power amplifier of the present invention.

Figure 12 is a schematic diagram of an embodiment of a power amplifier of the present invention having a preamplifier circuit.

Figure 13 is a timing diagram illustrating the voltages present in the amplifier shown in Figure 12.

Figure 14 is a schematic diagram of an embodiment of a two-stage differential power amplifier of the present invention.

Figure 15 is a schematic diagram of a prior art circuit used for performing differential-to-single-ended conversion.

15

Figure 16 is a block diagram of a differential-to-single-ended conversion and impedance transformation circuit of the present invention.

Figures 17 is a schematic diagram of a differential-to-single-ended conversion and impedance transformation circuit of the present invention.

20

Figures 18 and 19 are schematic diagrams illustrating differential inputs AC-coupled from a load.

Figure 20 is a block diagram of a differential-to-single-ended conversion and impedance transformation circuit having multiple differential inputs.

Figure 21 is a block diagram of a voltage regulator of the present invention.

Figure 22 is a schematic diagram of an embodiment of a voltage regulator of the present invention.

Figure 23 is a schematic diagram of an embodiment of a voltage regulator of the present invention.

Figure 24 is a schematic diagram of an embodiment of a voltage regulator of the present invention.

Figure 25 is an isometric view illustrating how a device of the present invention is packaged.

20

Figure 26 is a side view of the device shown in Figure 25.

Figure 27 is a diagram illustrating a ceramic chip carrier with an inductor formed in the carrier.

Figure 28 is a diagram illustrating a ceramic chip carrier with a vertically-formed inductor formed in the carrier.

5 Figure 29 is an electrical schematic diagram of inductors connected between four connection points.

Figure 30 is a diagram illustrating an example of how the inductors shown in Figure 29 could be formed in a ceramic chip carrier.

10

DETAILED DESCRIPTION

In order to provide a context for understanding this description, the following illustrates a typical application of the present invention. A power amplifier of the present invention may be used as an amplifier for use with a wireless transmission system such as a wireless telephone or other device. The invention may also be applied to other applications, including, but not limited to, RF power amplifiers. In a wireless device such as a cellular telephone, the device may include a transceiver, an antenna duplexer, and an antenna. Connected between the transceiver and the antenna duplexer is an RF power amplifier for amplifying signals for transmission via the antenna. This is one example of an application of a power amplifier of the present invention. Of course the invention may be used in any other application requiring a power amplifier. In the case of a wireless telephone application, the invention may be applied to GSM or other constant envelope modulation systems.

15

20

Figure 3 is a block diagram illustrating an example of an environment in which a power amplifier of the present invention may be used. Figure 3 shows a power amplifier 310 connected to a pair of input signals V_{in} and V_{ip} . The input signals come from an input 312 from an input network such as the transceiver chip mentioned above. An input buffer is formed by a plurality of inverters X1 and X2 which are connected to the input 312 as shown. The input buffer circuit could also be comprised of more or less inverters, or any other suitable circuitry. The power amplifier 310 is also connected to a voltage regulator 314 which provides a regulated voltage source V_{dd} from a voltage source, such as battery voltage VB. The power amplifier 310 is also connected to a transformation network 316 which is connected to a load 318. Note that the connection between power amplifier 310 and the transformation network 316 may be comprised of a single or multiple connections. Figure 3 is shown with n connections. In the example of a wireless transmission system, the load 318 may be comprised of an antenna. Note that the components shown in Figure 3 are optional and are not essential to the power amplifier 310.

Figure 4 is a schematic diagram of one embodiment of a power amplifier of the present invention. The power amplifier includes a switching device M1 connected between ground and the node labeled V_{dn} . The gate of the switching device M1 is connected to the input signal V_{in} . Another switching device M2 is connected between the voltage source V_{dd} and a node labeled V_{dp} . The gate of the switching device M2 is connected to the input signal V_{ip} . Connected between the switching devices M2 and M1

is an inductor L1. Figure 4 also shows a capacitor C1 connected between V_{dn} and ground. A capacitor C3 is connected between V_{dp} and Vdd. The capacitors C1 and C3 may be comprised of a combination of separate capacitors and parasitic capacitances of the switching devices M1 and M2. The power amplifier shown in Figure 4 also includes
 5 a reactive network connected between V_{dn} and the amplifier output V_o . The reactive network is formed by inductor L2 and capacitor C2 and can be used for filtering or impedance transformation. A load R_L is connected to the amplifier output V_o .

The power amplifier shown in Figure 4 resembles a push-pull amplifier
 10 topologically, but is fundamentally different, in that the input signals V_{in} and V_{ip} are inverses of one another. Since switching device M1 is an n-channel device and switching device M2 is a p-channel device, the switching devices M1 and M2 are both turned on and turned off during the same time intervals. Figure 5 is a timing diagram illustrating the voltages present in the amplifier shown in Figure 4, relative to the input signals.
 15 Figure 5 shows the input signals V_{in} and V_{ip} which are 180° out of phase with each other. In other words, when one of the input signals is high, the other is low. During phase 1 (V_{in} high and V_{ip} low), the switching devices M1 and M2 are both turned on so that V_{dp} and V_{dn} are clamped to Vdd and ground respectively. During phase 2 (V_{in} low and V_{ip} high), the switching devices M1 and M2 are both turned off. The voltage at V_{dn} rises and
 20 begins to ring at a frequency determined by the values of the components L1, C1, C3, L2, and C2. For the best efficiency, these components are chosen so that V_{dn} rises and then returns to ground immediately before the end of phase 2. The voltage at V_{dp} falls and

rings in a similar way. The voltage at node V_{dp} rises back to V_{dd} immediately before the end of phase 2, when switching devices M1 and M2 are turned on.

The peak voltages present across the switching devices M1 and M2 can be
5 adjusted as desired by changing the passive component values in the circuit under the constraint that the average voltage of V_{dn} must equal that of V_{dp} . If this average voltage lies at $V_{dd}/2$ then the peak value of V_{dn} will be only slightly higher than V_{dd} and that of V_{dp} will be only slightly lower than ground. The duty cycle of the input signals V_{in} and V_{ip} waveforms can be adjusted to reduce the peak voltages even further. As a result, this
10 configuration eliminates the large signal swings that transistors are subjected to in the prior art.

The power amplifier shown in Figure 4 does not take full advantage of the signal swing that occurs on node V_{dp} . An increase in efficiency can be achieved by making use
15 of the signal swing on both V_{dp} and V_{dn} . This can be accomplished by connecting the load differentially across nodes V_{dp} and V_{dn} as shown in Figure 6. Figure 6 shows a power amplifier similar to that shown in Figure 4. The power amplifier includes switching devices M1 and M2, inductor L1, and capacitors C1 and C3. A transformation network 616 is connected to both nodes V_{dp} and V_{dn} . A load R_L is connected to the
20 transformation network 616. The waveforms for the power amplifier shown in Figure 6 are similar to those for the power amplifier shown in Figure 4. In this embodiment, the

current flowing through the load R_L is determined by the difference between the voltages on V_{dp} and V_{dn} .

When a single-ended load is required, the transformation network can be made to
5 facilitate a single-ended load. Figure 7 shows a power amplifier with two capacitors C2 and C4 and an inductor L3 connected as shown between V_{dn} and V_o . An inductor L2 is connected between V_{dp} and the connection point of the capacitors C2 and C4. A single-ended load R_L is connected between V_o and ground. The waveforms for the power amplifier shown in Figure 7 are similar to those for the power amplifier shown in Figure
10 4. In this embodiment, the current flowing to the output from V_{dp} and current flowing to the output from V_{dn} add when they are summed in phase at the load. The load is AC coupled from either V_{dp} or V_{dn} by capacitor C4. The inductor L2 and capacitor C2 can also be chosen to transform the load impedance R_L into a desired impedance so that power delivered to the load can be adjusted independently from the voltage swing on V_{dp}
15 and V_{dn} . In this case, the voltage swing on V_o will vary from that on V_{dp} and V_{dn} as determined by the selection of C2 and L2. . Since the combination of L2 and C2 is a tuned circuit, it provides some bandpass filtering. If additional filtering is desired, capacitor C4 and inductor L3 can also be used as an additional bandpass filter. In summary, L2 and C2 in the configuration of Figure 7 simultaneously perform the
20 functions of impedance transformation, filtering, and differential-to-single-ended conversion.

The amplifier of the present invention may also be implemented differentially using two amplifiers (such as the amplifier shown in Figure 7) connected together as shown in Figure 8. Figure 8 shows a first amplifier (the positive side) comprised of switching devices M1+ and M2+, inductor L1+, capacitors C1+ and C3+, and a transformation network comprised of capacitors C2+ and C4+ and inductors L2+ and L3. A second amplifier (the negative side) is comprised of switching devices M1- and M2-, inductor L1-, capacitors C1- and C3-, and a transformation network comprised of capacitors C2- and C4- and inductors L2- and L3. The two amplifiers are similar to each other with the inductors L2 and capacitors C2 interchanged as shown. The input signals V_{in-} and V_{ip-} on the negative side are shifted by 180 degrees from the input signals V_{in+} and V_{ip+} on the positive side. Figure 9 is a timing diagram illustrating the voltages present at the nodes V_{dn+} , V_{dp+} , V_{dn-} and V_{dp-} .

The values of the passive components in the amplifier shown in Figure 8 may be chosen so that the resulting currents from both amplifiers sum in phase at the load R_L . The advantages of the power amplifier shown in Figure 8 are similar to the advantages common to differential circuits in general. For example, undesired interference from supply or substrate noise is common-mode. Another advantage is that the impact of supply resistance is reduced because the supply current flows during both clock phases.

20

Note that the load R_L shown in Figure 8 could be connected to only two of the four output nodes of the power amplifier. For example, a configuration similar to that

shown in Figure 4 could be connected differentially to the load R_L , where the nodes V_{dp+} and V_{dp-} are not connected to V_o .

Figure 8 also shows an alternate embodiment where an optional inductor $L4$ is
5 connected (shown in dashed lines) between nodes V_{dp+} and V_{dp-} . Without the optional inductor $L4$, the voltage swings on nodes V_{dp+} , V_{dp-} , V_{dn+} and V_{dn-} and the values of capacitors $C1+$, $C1-$, $C3+$ and $C3-$ can not be independently adjusted. The optional inductor $L4$ has the advantage that these voltage swings can be adjusted independently of the capacitance values mentioned above.

10

The capacitors $C1$ and $C3$ described above are used to shape the waveforms of the voltages on V_{dp} and V_{dn} . As mentioned above, these capacitances may be provided by separate capacitors or by the parasitic capacitances of switching devices $M1$ and $M2$. In another embodiment, these capacitances are formed by switching devices in a way that
15 improves the efficiency of the amplifier.

Figure 10 is a schematic diagram of a power amplifier similar to the amplifier shown in Figure 8. In the amplifier shown in Figure 10, the capacitors $C1+$ and $C3+$ are replaced by switching devices $M3-$ and $M4-$, respectively. Similarly, the capacitors $C1-$
20 and $C3-$ are replaced by switching devices $M3+$ and $M4+$, respectively. Each of the switching devices $M3$ and $M4$ are driven as shown by a voltage from the opposite amplifier. For example, the switching device $M4+$ is driven by the voltage at V_{dp-} on the

negative side. The switching device M4- is driven by the voltage at V_{dp+} on the positive side. Similarly, the switching device M3+ is driven by the voltage at V_{dn-} while the switching device M3- is driven by the voltage at V_{dn+} . The waveforms for the amplifier shown in Figure 10 are similar to those described above.

5

The amplifier shown in Figure 10 allows the switching devices M1+ and M1- to be made smaller by an amount equal to the size of switching devices M3+ and M3-. Similarly, the switching devices M2+ and M2- can be made smaller by an amount equal to the size of switching devices M4+ and M4-. However, switching devices M1 and M2 should remain sufficiently large to assure stability of the circuit. A decrease in the size of the switching devices M1 and M2 improves the efficiency since the input capacitances that must be driven are smaller. Another advantage to the amplifier shown in Figure 10 is that cross-coupling helps to assure that the waveforms present at V_{dp-} and V_{dn-} have the correct phase relationship to the waveforms present at V_{dp+} and V_{dn+} , despite possible timing variations on the positive inputs (V_{ip+} , V_{in+}) and on the negative inputs (V_{ip-} , V_{in-}).

15

Figure 10 also shows an alternate embodiment where an optional inductor L4 is connected (shown in dashed lines) between nodes V_{dp+} and V_{dp-} , similar to the inductor L4 shown in Figure 8. If the optional inductor L4 is connected, the voltage swings of nodes V_{dp+} , V_{dp-} , V_{dn+} , and V_{dn-} can be chosen independently from the input capacitances of M4-, M4+, M3-, M3+.

20

Figure 11 is a schematic diagram of a power amplifier similar to the amplifier shown in Figure 10, but with the inductors L1+ and L1- replaced. Inductor L1+ is replaced with a pair of inductors L1A+ and L1B+. Inductor L1- is replaced with a pair of inductors L1A- and L1B-. The node formed by the connection of inductors L1A+ and L1B+ is connected to the node formed by the connection of inductors L1A- and L1B-. The embodiment shown in Figure 11 has similar advantages to the embodiment in Figure 10 with the optional inductor L4 in that it allows the voltage swings of nodes Vdp+, Vdp-, Vdn+, and Vdn- to be chosen independently from the input capacitances of M4-, M4+, M3-, M3+.

10

As described above with respect to Figure 3, input buffer circuitry may be used to drive the gates of the switching devices M1 and M2 of the amplifiers described above. However, the efficiency may be improved if a similar amplifier circuit is used as a preamplifier circuit. Figure 12 is an example of an amplifier having a preamplifier circuit.

15

Figure 12 shows an amplifier similar to the amplifier shown in Figure 7. At the input of the amplifier, a preamplifier is shown. The preamplifier is comprised of switching devices M5 and M6 connected between ground and V_{dd}. An inductor L3 is connected between the switching devices M5 and M6. The preamplifier includes inputs V_{ip2} and V_{in2}. The preamplifier circuit receives input signals V_{ip2} and V_{in2} and generates signals V_{ip} and V_{in} for use by the amplifier. The preamplifier circuit is similar to the

20

amplifiers described above, except that all of the passive elements except inductor L3 are eliminated. The capacitances required by the preamplifier circuitry are formed from the input capacitances of the gates of switching devices M1 and M2. Of course, other passive elements could be used with the preamplifier circuit.

5

Figure 13 is a timing diagram illustrating the waveforms at V_{in} , V_{ip} , V_{dn} , and V_{dp} of Figure 12. The preamplifier output waveforms V_{ip} and V_{in} have a shape that makes them well suited for driving the input gates of switching devices M1 and M2 in the final stage.

10

Note that in an alternate configuration the capacitor C4 could be connected between inductor L2 and V_o with capacitor C2 connected between V_{dn} and V_o . This alternate configuration functions similarly to the configuration shown in Figure 12.

15

Figure 14 is a schematic diagram of an amplifier using a two-stage differential configuration which provides an increased efficiency over the circuit shown in Figure 12. The amplifier shown in Figure 14 is similar to the differential amplifier shown in Figure 10, with the addition of preamplifier circuitry. The inputs V_{ip+} and V_{in+} of the amplifier are connected to preamplifier circuitry comprised of switching devices M5+ and M6+.

20

The switching devices M5+ and M6+ are connected between ground and V_{dd} , with an inductor L3+ connected between them. Capacitances are provided to nodes V_{dp2+} and V_{dn2+} by switching devices M8+ and M7+, respectively. The negative side of the

amplifier is configured in the same manner. The positive and negative sides of the preamplifier circuitry are cross-coupled in the same way as the amplifier circuitry shown in Figure 10 (described above). In this configuration, the input capacitances of the NMOS and PMOS switching devices M1 and M2 of the power amplifier, the input
5 capacitances of the preamplifier switching devices M7 and M8, and the value of inductor L5 can be adjusted so that the signals at V_{dp2} and V_{dn2} have the desired peak amplitudes.

Another aspect of the present invention relates to a circuit and method of providing differential-to-single ended output conversion and impedance transformation
10 from differential signals. Differential circuits have a number of advantages that are well known. For example, the impact from noise sources is reduced since these signals are common-mode (i.e., the positive and negative sides are effected identically). In addition, even-order harmonics are reduced because of circuit symmetry. Because of these and other advantages, a differential configuration may be desirable even when the load is
15 single-ended. If a single-ended load is needed, circuitry for differential-to-single-ended conversion is needed.

One prior art method for performing differential-to-single-ended conversion at high frequency involves use of a transformer or balun. Figure 15 shows a prior art circuit
20 used for performing differential-to-single-ended conversion using a transformer T1. The primary side of the transformer T1 is connected to a first differential input V_+ and a second differential input V_- . The secondary side of the transformer T1 is connected to

ground and an output node V_O . A load Z_L is connected between ground and the output node V_O . If the transformer has a 1-to-1 turns ratio, then the differential signals V_+ and V_- are translated into a signal having an amplitude of $(V_+ - V_-)$ across the load Z_L .

5 In some applications, impedance matching or impedance transformation is needed to transform a given load impedance into a different impedance seen by the driver. Impedance transformation can be accomplished, as part of the differential-to-single ended conversion, using the transformer circuit shown in Figure 15 by adjusting the winding ratio of the transformer T1. However, the use of transformers for differential-to-single-
10 ended conversion and impedance transformation has disadvantages. First, high quality transformers are larger and more costly than other passive elements and are not easily integrated with other semiconductor circuits. Second, practical transformers have imperfect magnetic coupling which causes a loss of power from input to output.

15 The present invention provides a technique that performs differential-to-single ended conversion as well as impedance transformation and avoids the disadvantages of a transformer solution. Figure 16 shows a block diagram of a differential-to-single-ended conversion and impedance transformation circuit. The circuit has a first impedance X_1 coupled between the second differential input signal V_- and an output node V_O . A second
20 impedance X_2 is coupled between the first differential input signal V_+ and the output node V_O . A load Z_L is connected between the output node V_O and ground. In the circuit shown in Figure 16, current flowing to the output node V_O from differential input V_+ is

shifted in phase from the voltage on V_+ . Similarly, current flowing to the output node V_O from differential input V_- is shifted in phase from the voltage on V_- . The impedances X_1 and X_2 are chosen so that these two currents add together when they are summed at the load Z_L . For example, if X_1 shifts the output current by $+90$ degrees and X_2 shifts the output current by -90 degrees then the resultant currents will sum in phase at the load. Figure 17 illustrates one example of an implementation of the circuit shown in Figure 16. Figure 17 shows an L-C differential-to-single-ended conversion and impedance transformation circuit. The impedance X_1 is comprised of a capacitor C_5 which is coupled between the second differential input signal V_- and the output node V_O . The impedance X_2 is comprised of an inductor L_6 which is coupled between the first differential input signal V_+ and the output node V_O .

Referring back to Figure 16, since the inputs V_+ and V_- are differential, the inputs have opposite signs. However, the differential inputs V_+ and V_- are not necessarily equal in amplitude. The output voltage V_O of the differential-to-single-ended conversion and impedance transformation circuit is given by the following equation:

$$V_O = \frac{(V_+ X_1 + V_- X_2)(-jX_2 X_1 + (X_1 + X_2)Z_L)}{((X_1 X_2)^2 + (X_1 + X_2)^2 Z_L^2)} Z_L. \quad (1)$$

The power P_L delivered to the load Z_L is given by the following equation:

$$P_L = \frac{(V_+ X_1 + V_- X_2)^2}{((X_1 X_2)^2 + (X_1 + X_2)^2 Z_L^2)} Z_L. \quad (2)$$

Differential-to-single-ended conversion is achieved if the impedances X_1 and X_2 have opposite signs. Impedances X_1 and X_2 may be comprised of any combination of reactive elements (e.g., capacitor C5 and inductor L6 shown in Figure 17) whose combination meets this requirement. For example, if differential inputs V_+ and V_- have equal

5 amplitudes A , and impedances X_1 and X_2 have equal amplitudes X , then the output voltage V_o can be determined by substituting these values into equation (1) above. The resulting output voltage V_o is given by the following equation:

$$V_o = -j2A \frac{Z_L}{X}. \quad (3)$$

10 It can be seen from equation (3) that the ratio R/X can be chosen so that the amplitude of the output V_o is either larger or smaller than the amplitude A of the differential input. The voltage of the output V_o increases as the value of X decreases. Similarly, the voltage of the output V_o decreases as the value of X increases.

15 In certain applications, the load Z_L must be AC-coupled from one of the differential inputs V_- or V_+ . Figures 18 and 19 show examples of how the differential inputs may be AC-coupled from the load Z_L in the example shown in Figure 17. In the circuit shown in Figure 18, an additional capacitor C6 is inserted between the output node V_o and both the capacitor C5 and the inductor L6. The capacitor C6 AC-couples the

20 output node V_o from the first and second differential inputs V_+ and V_- . In the circuit

shown in Figure 19, an additional capacitor C6 is inserted between the output node V_o and the inductor L6. The capacitor C6 AC-couples the output node V_o from the first differential input V_+ . Note that the capacitor C1 provides AC-coupling between the output node V_o from the second differential input V_- .

5

The techniques for providing differential-to-single-ended conversion and impedance transformation described above can be applied to circuits having multiple differential inputs. Figure 20 shows a differential-to-single-ended conversion and impedance transformation circuit having multiple differential inputs. Figure 20 shows differential inputs V_1 through V_N , where N is the total number of differential inputs. A first impedance X_1 is coupled between the differential input V_1 and the output node V_o . A second impedance X_2 is coupled between the differential input V_1 and the output node V_o . Similarly, an N th impedance X_N is coupled between the differential input V_N and the output node V_o . Each of the currents from each differential input is summed in phase at the output node V_o . In this embodiment, the impedance X_j between the j th differential input V_j and the output node V_o will depend on its phase with respect to that of other differential inputs. Optimal power transfer to the load Z_L occurs when the impedances X_j are purely reactive. However, this technique may still be applied when impedance X_j is not purely reactive. For example, this might occur when actual inductors and capacitors have a series resistance.

20

As mentioned above, the RF power amplifier shown in Figure 3 includes a voltage regulator 314 connected between the power amplifier 310 and a source of battery voltage VB to provide a voltage source VDD. In one embodiment of the present invention, the voltage regulator 314 resides on the same integrated circuit as the power amplifier circuit. The function of the voltage regulator is to provide a source of voltage to the power amplifier and to help control the output power level. For example, in a cellular phone environment, a base station may dictate the power level at which each cell phone should transmit (based on factors such as the physical distance from the base station, for example). Varying the voltage level (VDD) can control the output power of the power amplifier. As the voltage of the voltage source VDD increases, the output power increases. Therefore, by controlling the operation of the voltage regulator, and therefore controlling the voltage of voltage source VDD, the output power of the amplifier can be controlled. While the power amplifier 310 will function with any suitable voltage regulator or voltage source, described below is a detailed description of a suitable voltage regulator.

Figure 21 is a block diagram of a voltage regulator 544 used to provide a regulated voltage VDD from a voltage source VB, for example, from a battery. As shown, the regulated voltage VDD is provided to a device 530. The device 530 may be any type of device requiring a voltage source including, but not limited to power amplifiers. The voltage regulator 544 includes an input 546 that is connected to a control signal VSET to control the voltage level VDD provided to the device 530. Following is a detailed description of the voltage regulator of the present invention in the context of its use in an RF power amplifier (such as that shown in Figure 3). However, it is understood that the voltage regulator may be used with any type of amplifier as well as any other type of device requiring a voltage source.

Figure 22 is a schematic diagram of a first embodiment of a voltage regulator 644 connected to a battery voltage VB. The voltage regulator 644 is comprised of a device M9 and an op amp X4. The op amp X4 includes a first input 646 for connection to a voltage control signal VSET. In a preferred embodiment, the control signal VSET is an analog voltage signal that is proportional to the desired voltage level. The other input to the op amp X4 is connected to the regulated voltage VDD. The output of the op amp X4 is connected to the input of the device M9.

Figure 23 is a schematic diagram of another embodiment of a voltage regulator 744 connected to a battery voltage VB. The voltage regulator 744 is similar to the voltage regulator 644 shown in Figure 22 with the addition of a second regulator circuit comprised of op amp X5, switching device M10, and an external resistor R1. Figure 23 also shows an integrated circuit 770 (dashed lines) to illustrate that the power amplifier is formed on the integrated circuit 770 while the resistor R1 is not. The integrated circuit 770 may also be the same integrated circuit on which the device to be powered resides.

The first regulator circuit is connected in the same manner as the regulator circuit shown in Figure 22. The op amp X5 of the second regulator circuit includes an input VSET2 for connection to a voltage control signal. The other input to the op amp X5 is connected to the regulated voltage VDD. The output of the op amp X5 is connected to the gate of the device M10. The external resistor R1 is connected between the battery voltage VB and the device M10. Figure 23 also shows voltage control circuitry 776 which has an input 746 connected to the control signal VSET. The voltage control circuitry 776 uses the signal VSET to create voltage control signals VSET1 and VSET2 for use by the first and second regulator circuits. By controlling both regulators, the

voltage level VDD can be controlled. In addition, by selectively activating the second regulator, power can be dissipated off the integrated circuit 770 (via resistor R1). This results in a reduction of heat generated in the integrated circuit 770.

5 The voltage regulator 744 operates as follows. Since it is desired to minimize the amount of power dissipated on the integrated circuit 770, one goal is to maximize the use of the second regulator circuit (X5, M10) in order to maximize power dissipation through the external resistor R1. Therefore, voltage control circuitry 776 will enable the second
10 circuit (X4, M9). In other words, when more power is required than the second regulator circuit can provide, the first regulator circuit is enabled to provide additional power. In this way, the maximum amount of power will be dissipated through external resistor R1.

Figure 24 is a schematic diagram of another embodiment of voltage regulator 844
15 having multiple regulators and multiple external resistors. The voltage regulator 844 is similar to the regulator 744 shown in Figure 23, with the addition of a third regulator circuit comprised of device M11, op amp X6, and external resistor R2. The third regulator circuit is connected in the same ways as the second regulator circuit, and operates in a similar manner. The op amp X6 of the third regulator circuit includes an
20 input VSET3 for connection to a voltage control signal. The other input to the op amp X5 is connected to the regulated voltage VDD. The output of the op amp X6 is connected to the gate of device M11. The external resistor R2 is connected between the batter voltage VB and device M11. Figure 24 also shows voltage control circuitry 876 which has an input 846 connected to the control signal VSET. The voltage control
25 circuitry 876 uses the signal VSET to create voltage control signals VSET1, VSET2, and VSET3 for use by the regulator circuits. By activating the second or third regulator,

power can be dissipated off the integrated circuit 870 (via resistor R1 and/or R2). This results in a reduction of heat generated in the integrated circuit 870.

The voltage regulator 844 operates as follows. Since it is desired to minimize the amount of power dissipated on the integrated circuit 870, one goal is to maximize the use of the second and third regulator circuits in order to maximize power dissipation through the external resistors R1 and R2. Therefore, voltage control circuitry 876 will enable the second and third regulator circuits to provide as much power as it can before enabling the first regulator circuit. In other words, when more power is required than the second and/or third regulator circuit can provide, the first regulator circuit is enabled to provide additional power. In this way, the maximum amount of power will be dissipated through external resistors R1 and R2.

The values of the resistors R1 and R2 may be equal, or may be different, depending on the needs of a user. In addition, the invention is not limited to the use of one or two external resistors. Additional regulator circuits and external resistors could be added. In one embodiment, the value of resistor R1 is 0.7 ohms and the value of resistor R2 is 0.3 ohms.

Another benefit of the present invention involves the use of dual gate oxide devices. In CMOS digital systems, it is sometimes desired to provide devices suitable for use with two voltage levels (e.g., 3.3 volts and 5 volts). Therefore, processing technologies have been developed to provide a single integrated circuit having both 0.5 μm and 0.35 μm devices. As mentioned above, a thicker gate oxide results in a device with a higher breakdown voltage. On the other hand, a thinner gate oxide results in a faster device, but with a lower breakdown voltage.

The RF amplifier of the present invention takes advantage of the availability of dual gate oxide devices by selectively choosing certain gate lengths for various components of the amplifier. For example, it has been discovered that for preprocessing circuitry or pre-driver circuitry, a high speed is desirable and breakdown voltage is not as important. Therefore these devices are designed using a thinner gate oxide. For output state devices, where a high breakdown voltage is more important, the devices are designed using a thicker gate oxide.

10 In one embodiment, a dual gate oxide device is used to create an RF amplifier such as the RF amplifier shown in Figures 12, and 14. One suitable use of dual gate oxides in these amplifiers is to utilize devices having channel lengths of both 0.5 μm and 0.35 μm . The 0.5 μm and 0.35 μm devices have gate oxide thicknesses of 140 Angstroms (\AA) and 70 \AA , respectively. Referring to the example shown in Figure 12, the predriver devices M5 and M6 can be chosen with much smaller device widths than the output devices M1 and M2. In this case, the predriver output signals V_{ip} and V_{in} are nearly sinusoidal, the voltage difference ($V_{ip}-V_{in}$) varies between about $+V_{dd}$ and $-V_{dd}$, and the input capacitances of M1 and M2 can be chosen so that neither M5 nor M6 experiences a voltage drop that is larger than V_{dd} . As a result, a high breakdown voltage is not critical for the predriver and devices M5 and M6 can be implemented using 0.35 μm devices. When high efficiency is desired, switching devices M1 and M2 of the final amplifier stage are sized with large device widths so that nodes V_{dn} and V_{dp} are strongly clamped to their respective supply voltages of ground and V_{dd} when these devices are on. In this case, the voltage difference ($V_{dp}-V_{dn}$) varies over a range that is larger than that of the predriver and either M1, M2, or both will experience a voltage drop that is larger than V_{dd} . Since a higher breakdown voltage is desired from these devices, M1

and M2 can each be implemented using 0.5 μm devices. Since PMOS transistors are typically slower than NMOS transistors and thicker gate oxide devices are slower than thinner gate oxide devices, it is preferable to use a thicker gate oxide for NMOS devices than for PMOS devices. An example of the use of dual gate oxide thicknesses for the RF amplifier of Figure 14 includes only NMOS devices with a thick gate oxide. Predriver transistors M5+, M5-, M6+, M6-, M7+, M7-, M8+, and M8- are implemented using using 0.35 μm devices because, as described above, they are not subjected to voltage drops greater than Vdd and breakdown is not a critical concern. As described above, the final amplifier stage experiences larger voltage swings. However these larger swings can be distributed across across its NMOS and PMOS devices in such a way that only NMOS devices see a voltage swing larger than Vdd. This is accomplished by adjusting the values of inductors L1+, L1-, and L4 and the input capacitances of devices M3+, M3-, M4+, and M4-. In this approach, PMOS devices M2+, M2-, M4+, and M4- in the final amplifier stage are thinner gate oxide devices, whereas NMOS devices M1+, M1-, M3+, M3- are thicker gate oxide devices.

Of course, the present invention is not limited to the values described above. For example, as thinner gate oxides become more common, one or both thicknesses may become lower. In addition, note that the terms "thicker" or "thinner" in this description are intended to only refer to intentional or significant differences in gate oxide thicknesses. For example, the 0.35 μm devices may vary from one another by some small amount depending on manufacturing tolerances. A 0.5 μm device is considered to be "thicker" than a 0.35 μm device. Also note that this invention applies to various CMOS devices and that the RF Amplifier described above is only used as one example of the application of dual gate oxide devices of the present invention.

Another benefit of the present invention relates to how an RF power amplifier of the present invention is packaged. The design of an RF amplifier requires a low inductance and low resistance to the transistors or switching devices. In addition, RF power amplifier designs typically require a number of passive components such as inductors and capacitors. It is advantageous to integrate these components in the power amplifier package. The packaging technique of the present invention addresses these concerns by using "flip chip" technology and multi-layer ceramic chip carrier technology.

Figures 25 and 26 are isometric and side views, respectively, illustrating a packaging technique of the present invention. Figures 25 and 26 show a "flip chip" integrated circuit 970 mounted to a multi-layer ceramic chip carrier 972. The integrated circuit 970 includes a plurality of connection points, or "bumps" 974 on the underside of the integrated circuit 970. Similarly, the ceramic chip carrier 972 includes a plurality of connection points or bumps 976. The bumps 974 of the integrated circuit 970 are formed by solder and can be mounted to corresponding conductive material formed on the upper surface of the ceramic chip carrier 972. Similarly, the bumps 976 of the ceramic chip carrier 972 are also formed by solder and are used to mount the chip carrier 972 to a printed circuit board (not shown). A typical flip chip allows 250 μm spaced bumps. A typical chip carrier also allows 250 μm spaced vias for connection to the flip chip bumps. In one example, 6x6 mm ceramic chip carrier includes 36 bumps 976 for connection to a PCB. Flip chip and ceramic chip carrier technologies are considered conventional and will not be described in detail.

Various benefits can be realized by selectively placing certain components of the RF power amplifier of the present invention on integrated circuit 970 and ceramic chip carrier 972. The invention will be described with respect to the RF power amplifier

shown in Figure 14, although the invention is not limited to power amplifiers. In one embodiment of the invention, all of the switching devices are formed on the integrated circuit 970. In addition, the power transistors (such as switching devices M1+, M1-, M2+, M2-) formed on the integrated circuit 970 are preferably placed directly below the
5 bumps 974 of the integrated circuit 970 resulting in low resistance and inductance (as compared to wire bond integrated circuit packages).

The multi-layer ceramic chip carrier 972 is used to build high-Q inductors, transformers, and capacitors. This can be beneficial for CMOS power amplifier
10 architecture since multiple inductors and capacitors may be required. For example, a single band power amplifier may require 4-8 inductors which would be impractical to build on a printed circuit board. In addition, multiple matching networks are used to provide the high transformation ratio required in a push-pull amplifier design. In one embodiment of the invention, the transformers, inductors, capacitors, and other passive
15 devices are formed on the ceramic chip carrier 972. The ceramic chip carrier 972 includes multiple conductive layers 978 (shown as hidden lines) that can be designed to implement these passive devices.

In one embodiment of the RF power amplifier shown in Figure 14, all of the
20 switching devices and capacitors C2+ and C2 reside on the integrated circuit 970, with the inductors L3+, L3-, L5, L1+, L1-, L4, L2+, and L2- residing on the multi-layer ceramic chip carrier 972.

In a CMOS power amplifier design, multiple high-Q inductors are required to
25 tune out large on-chip gate capacitances. Since these capacitances are large, the required inductors are low in value and difficult to integrate. One solution is to form high-Q

inductors on the ceramic chip carrier. Figure 27 is a diagram illustrating the ceramic chip carrier 972 shown in Figures 25 and 26 with a horizontally-formed inductor 1180 formed in the ceramic chip carrier 972. The inductor 1180 includes a horizontal loop portion formed by conductive trace 1182 connected to two bumps 974 of the ceramic chip carrier 972 by two vias 1184. One disadvantage with the inductor 1180 is that the inductor connection points need to be close to the edge of the ceramic chip carrier 972 unless the value of the inductor is large enough to route to a lower layer of the ceramic chip carrier 972.

Figure 28 is a diagram illustrating the ceramic chip carrier 972 with a vertically-formed inductor 1280 formed in the carrier 972. The inductor 1280 is formed in the vertical direction by vias 1284 extending to conductive trace 1286, which may be formed on a lower level of the carrier 972. As shown, the inductor 1280 extends downward into the ceramic chip carrier 972 and is coplanar, since the vias 1284 and trace 1286 exist on the same plane. The vias 1284 may be formed through several layers of the carrier 972, depending on the inductance desired. A vertically-formed inductor such as the inductor 1280 has two major advantages over horizontally-formed inductors. First, the vertically-formed inductors can be formed underneath the chip 970 without blocking other routing channels. Therefore, more layout options are available, and more inductors can be formed. Second, the vertically-formed vias 1284, as opposed to the horizontal conductive trace 1182, result in less loss at RF frequencies since the vias 1284 have a greater cross-sectional surface area than the conductive traces. The vias 1284 are substantially cylindrical and have a surface area of πdL , where d is the diameter of the via 1284 (e.g., 100 μm) and L is the length of the via. The conductive traces, such as conductive trace 1182, have a surface area of $2dL$. Therefore, the resistance of a via at RF frequencies is approximately $\pi/2$ less than the resistance of a conductive trace 1182.

- Figures 29 and 30 illustrate one embodiment of vertically-formed inductors of the present invention. Figure 29 is an electrical schematic diagram showing inductors L7, L8, L9, L10, and L11 connected between connection points 1310, 1312, 1314, and 1316. As shown, inductors L7 and L8 are connected between connection points 1310 and 1312. Similarly, inductors L9 and L10 are connected between connection points 1314 and 1316. Inductor L11 is connected between connection points 1318 and 1320, which are formed between inductors L9 and L10, and L7 and L8.
- Figure 30 illustrates an example of how the circuit of Figure 29 can be implemented using vertically-formed inductors of the present invention. The connection points 1310, 1312, 1314, and 1316 are formed at the surface of the ceramic chip carrier (not shown in Figure 30) and will be electrically connected to four of the bumps 974 of the flip-chip 970. In this example, the inductors are formed using the upper two layers of the ceramic chip carrier. Vias 1322 and 1324 extend through both layers where they are connected to an end of conductive traces 1326 and 1328, respectively, formed in the lower layer of the ceramic chip carrier. The opposite ends of the conductive traces 1326 and 1328 are connected to vias 1330 and 1332, respectively, which are also formed in the lower layer of the ceramic chip carrier. Together, the via 1322, conductive trace 1326, and via 1330 form inductor L7. Similarly, the via 1324, conductive trace 1328, and via 1332 form inductor L9. The vias 1330 and 1332 are connected to opposite ends of conductive trace 1334, formed in the upper layer. The conductive trace 1334 forms the inductor L11. Finally, vias 1336 and 1338 are connected to the vias 1330 and 1332, respectively, as well as to opposite ends of the conductive trace 1334. The vias 1336 and 1338 form the

inductors L8 and L10, respectively. While Figures 29 and 30 show one specific example of how inductors could be formed in the ceramic chip carrier, it should be understood that other implementations are possible.

- 5 In the preceding detailed description, the invention is described with reference to specific exemplary embodiments thereof. Various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

- 1 1. A power amplifier comprising:
2 a first switching device connected between a first supply voltage and a first output node;
3 a second switching device connected between a second supply voltage and a second
4 output node; and
5 an inductance coupled between the first and second output nodes.
- 1 2. The power amplifier of claim 1, wherein a load is coupled to the second output
2 node.
- 1 3. The power amplifier of claim 1, further comprising a first capacitor coupled to the
2 first output node, and a second capacitor coupled to the second output node.
- 1 4. The power amplifier of claim 1, further comprising a first capacitor coupled to the
2 first output node.
- 1 5. The power amplifier of claim 1, further comprising a first capacitor coupled
2 between the first and second output nodes.
- 1 6. The power amplifier of claim 1, wherein the first and second switching devices
2 are driven by signals that repeatedly turn the devices on and off.

1 7. The power amplifier of claim 6, wherein the first and second switching devices
2 are both cycled on during the same time period, and wherein the first and second
3 switching devices are both cycled off during the same time period.

1 8. The power amplifier of claim 4, wherein the first capacitor is provided by the
2 input capacitance of a third switching device.

1 9. The power amplifier of claim 3, wherein the first capacitor is provided by the
2 input capacitance of a third switching device, and wherein the second capacitor is
3 provided by the input capacitance of a fourth switching device.

1 10. The power amplifier of claim 1, wherein the first and second switching devices
2 are comprised of transistors.

1 11. The power amplifier of claim 1, wherein the first switching device is comprised of
2 a PMOS transistor, and wherein the second switching device is comprised of an NMOS
3 transistor.

1 12. The power amplifier of claim 1, further comprising a load coupled across the first
2 and second output nodes.

1 13. The power amplifier of claim 1, further comprising a transformation network
2 coupled to the first and second output nodes.

1 14. The power amplifier of claim 13, wherein the transformation network further
2 comprises:
3 a capacitor coupled to the first output node and a third node;
4 an inductor coupled to the second output node and the third node; and
5 a load coupled to the third node.

1 15. The power amplifier of claim 1, further comprising a preamplifier connected to
2 the power amplifier, the preamplifier further comprising:
3 a third switching device connected between said first supply voltage and a third node and
4 coupled to the input to the first switching device;
5 a fourth switching device connected between said second supply voltage and a fourth
6 node and coupled to the input to the second switching device; and
7 a second inductor coupled between the third and fourth nodes.

1 16. The power amplifier of claim 1, further comprising one or more inductors coupled
2 between the first output node and a third supply voltage.

1 17. The power amplifier of claim 1, further comprising one or more inductors coupled
2 between the first output node and a third supply voltage, and one or more inductors
3 coupled between the second output node and a fourth supply voltage.

1 18. A method of reducing the peak output voltage of an amplifier comprising the
2 steps of:
3 providing an inductor having first and second terminals;

4 providing a first switching device connected between the first terminal of the inductor
5 and a first supply voltage;
6 providing a second switching device connected between the second terminal of the
7 inductor and a second supply voltage;
8 applying a voltage between the first and second terminals of the inductor during a first
9 portion of a clock cycle by turning on the first and second switching devices; and
10 turning off the first and second switching devices during a second portion of the clock
11 cycle.

1 19. The method of claim 18, further comprising the steps of providing a first
2 capacitance connected to the first terminal, providing a second capacitance connected to
3 the second terminal, wherein current from the inductor charges or discharges the first and
4 second capacitances during the second portion of the clock cycle.

1 20. The method of claim 18, further comprising the step of connecting a load to the
2 first node.

1 21. The method of claim 18, wherein the load includes a reactive network.

1 22. The method of claim 18, further comprising the step of driving the first and
2 second switching devices such that the switching devices are turned on and off
3 simultaneously.

1 23. The method of claim 18, further comprising the step of driving the first and
2 second switching devices by repeatedly turning both devices on and then turning both
3 devices off.

1 24. The method of claim 18, wherein the switching devices are comprised of
2 transistors.

1 25. The method of claim 18, further comprising the step of differentially connecting a
2 load to the first and second nodes.

1 26. The method of claim 18, wherein the load is connected across the first and second
2 nodes.

1 27. The method of claim 18, further comprising the steps of:
2 providing a third switching device connected between the gate of the first switching
3 device and a third supply voltage;
4 providing a fourth switching device connected between the gate of the second switching
5 device and a fourth supply voltage; and
6 providing a second inductor connected between the gates of the first and second
7 switching devices.

1 28. A differential power amplifier comprising:
2 a first amplifier having a first switching device connected between a first supply voltage
3 and a first output node, a second switching device connected between a second
4 supply voltage and a second output node, and an inductance coupled between the
5 first and second output nodes;
6 a second amplifier having a third switching device connected between a third supply
7 voltage and a third output node, a fourth switching device connected between a

8 fourth supply voltage and a fourth output node, and an inductance coupled
9 between the third and fourth output nodes; and
10 wherein the first and second amplifiers are coupled together to drive a load.

1 29. The differential power amplifier of claim 28, wherein the second and fourth
2 output nodes of the first and second amplifiers are coupled together to drive the load.

1 30. The differential power amplifier of claim 28, wherein the first, second, third, and
2 fourth output nodes of the first and second amplifiers are coupled together to drive the
3 load.

1 31. The differential power amplifier of claim 28, further comprising:
2 a first transformation network connected between the first and second output nodes of the
3 first amplifier and the load, and
4 a second transformation network connected between the third and fourth output nodes of
5 the second amplifier and the load.

1 32. The differential power amplifier of claim 28, further comprising:
2 a first transformation network connected between the second output node of the first
3 amplifier and the load, and
4 a second transformation network connected between the third output node of the second
5 amplifier and the load.

1 33. The differential power amplifier of claim 28 further comprising:
2 an inductor coupled between the first output node and the third output node.

1 34. The differential power amplifier of claim 28 further comprising:
2 an inductor coupled between the second output node and the fourth output node.

1 35. The differential power amplifier of claim 31, wherein the first transformation
2 network further comprises:
3 a first capacitor coupled to the second output node of the first amplifier and coupled to
4 the load; and
5 a first inductor coupled to the first output node of the first amplifier and coupled to the
6 load.

1 36. The differential power amplifier of claim 31, wherein the second transformation
2 network further comprises:
3 a second capacitor coupled to the third output node of the second amplifier and coupled
4 to the load; and
5 a second inductor coupled to the fourth output node of the second amplifier and coupled
6 to the load.

1 37. The differential power amplifier of claim 28, wherein the first amplifier receives
2 first and second inputs.

1 38. The differential power amplifier of claim 37, wherein the first and second
2 switching devices of the first amplifier are enabled and disabled simultaneously; and
3 wherein the third and fourth switching devices of the second amplifier are enabled and
4 disabled simultaneously.

1 39. The differential power amplifier of claim 38, wherein the first and second
2 switching devices of the first amplifier are enabled during the time that the third and
3 fourth switching devices of the second amplifier are disabled, and wherein the third and
4 fourth switching devices of the second amplifier are enabled during the time that the first
5 and second switching devices of the first amplifier are disabled.

1 40. The differential power amplifier of claim 28, wherein the amplifier further
2 comprises:
3 a first capacitance coupled between the first output node and the first supply voltage;
4 a second capacitance coupled between the second output node and the first supply
5 voltage; and
6 wherein the second amplifier further comprises:
7 a third capacitance coupled between the third output node and a third supply voltage;
8 a fourth capacitance coupled between the fourth output node and a fourth supply
9 voltage.

1 41. The differential power amplifier of claim 40, wherein the first, second, third, and
2 fourth capacitances are provided by capacitors.

1 42. The differential power amplifier of claim 40 wherein the first, second, third, and
2 fourth capacitances are provided by the input capacitance of fifth, sixth, seventh, and
3 eighth switching devices, respectively.

1 43. The differential power amplifier of claim 42, wherein the fifth switching device is
2 coupled to the third output node, and the sixth switching device is coupled to the fourth

3 output node, and the seventh switching device is coupled to the first output node, and the
4 eighth switching device is coupled to the second output node.

1 44. The differential power amplifier of claim 28, further comprising a preamplifier for
2 each of the first and second power amplifiers.

1 45. The differential power amplifier of claim 44, wherein each of the preamplifiers
2 further comprise:
3 fifth and sixth switching devices connected between the first and second supply voltages;
4 and
5 a third inductor connected between the fifth and sixth switching devices.

1 46. The differential power amplifier of claim 28, wherein the first and second
2 amplifiers are cross-coupled.

1 47. A GSM RF power amplifier for wireless transmission comprising:
2 a plurality of RF amplifier stages implemented in a CMOS device; and
3 a plurality of passive components implemented on a carrier, wherein the carrier and the
4 CMOS device are packaged together to form the GSM RF power amplifier.

1 48. A circuit for providing differential-to-single ended conversion and impedance
2 transformation from first and second differential signals comprising:
3 a first impedance connected between the first differential signal and an output node; and
4 a second impedance connected between the second differential signal and the output
5 node, wherein the first and second impedances are comprised of reactive

6 elements, and wherein the first impedance has a positive sign and the second
7 impedance has a negative sign.

1 49. The circuit of claim 48, wherein the values of the first and second impedances are
2 chosen to transform a load impedance, connected to the output node, into a different
3 impedance at the differential inputs.

1 50. The circuit of claim 48, wherein the first impedance is comprised of a capacitor and
2 the second impedance is comprised of an inductor.

1 51. The circuit of claim 48, wherein the first impedance shifts the current delivered to a
2 load by -90 degrees from the first differential signal voltage and the second impedance shifts
3 the current delivered to the load by +90 degrees from the second differential signal voltage.

1 52. The circuit of claim 48, wherein the first impedance shifts the current delivered to a
2 load from the first differential signal voltage by a first amount in a first direction, and
3 wherein the second impedance shifts the current delivered to the load from the second
4 differential signal by a second amount in a second direction.

1 53. The circuit of claim 52, wherein the first and second shifts in the current delivered to
2 the load are 180 degrees apart.

1 54. The circuit of claim 48, further comprising a capacitor coupled between the output
2 node and a load to AC-couple the output node from one or more of the differential signals.

1 55. The circuit of claim 50, further comprising a capacitor coupled between the output
2 node and the second differential signal to AC-couple the output node from the second
3 differential signal.

1 56. The circuit of claim 48, further comprising a power amplifier for providing the first
2 and second differential signals.

1 57. A circuit for providing differential-to-single ended conversion and impedance
2 transformation from a plurality of differential input pairs, each differential input pair
3 comprising first and second signals, the circuit comprising:
4 a first impedance with a positive sign connected between the first signal of each differential
5 signal pair and an output node; and
6 a second impedance with a negative sign connected between the second signal of each
7 differential signal pair and the output node; and
8 wherein the first and second impedances are comprised of reactive elements.

1 58. The circuit of claim 57, further comprising a capacitor coupled between the output
2 node and a load to AC-couple the output node from one or more of the differential signals.

1 59. The circuit of claim 57, further comprising a capacitor coupled between the output
2 node and the second signal of one or more of the differential signal pairs to AC-couple the
3 output node from these second signals.

1 60. A differential-to-single ended conversion circuit comprising:
2 a first input node connectable to a first differential signal;

- 3 a second input node connectable to a second differential signal;
- 4 an output node for providing a single ended output;
- 5 a first impedance connected to the first input node and to the output node;
- 6 a second impedance connected to the second input node and to the output node; and
- 7 wherein the first impedance has a positive sign and the second impedance has a negative sign.

- 1 61. The differential-to-single ended conversion circuit of claim 60, wherein the first
- 2 impedance is comprised of a capacitor and the second impedance is comprised of an
- 3 inductor.

1/14

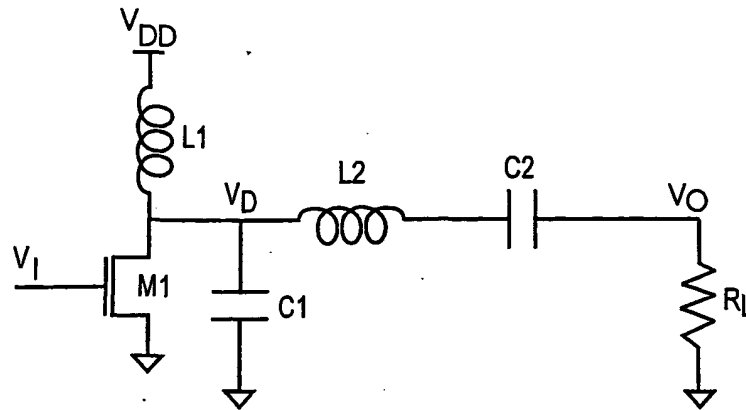
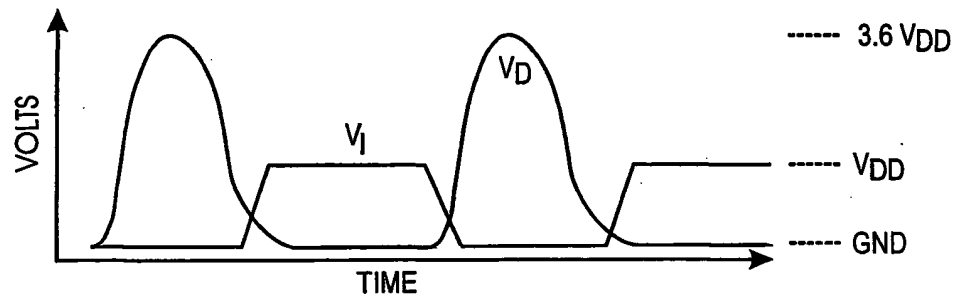
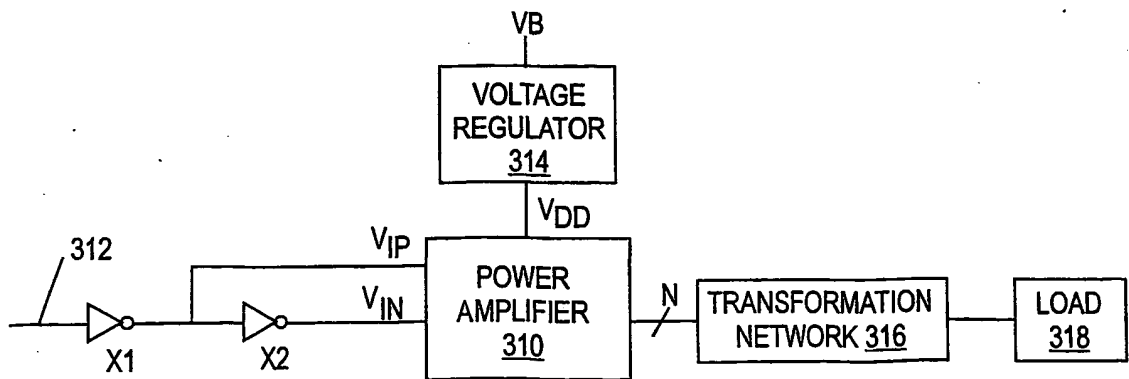
FIG. 1
(PRIOR ART)FIG. 2
(PRIOR ART)

FIG. 3

2/14

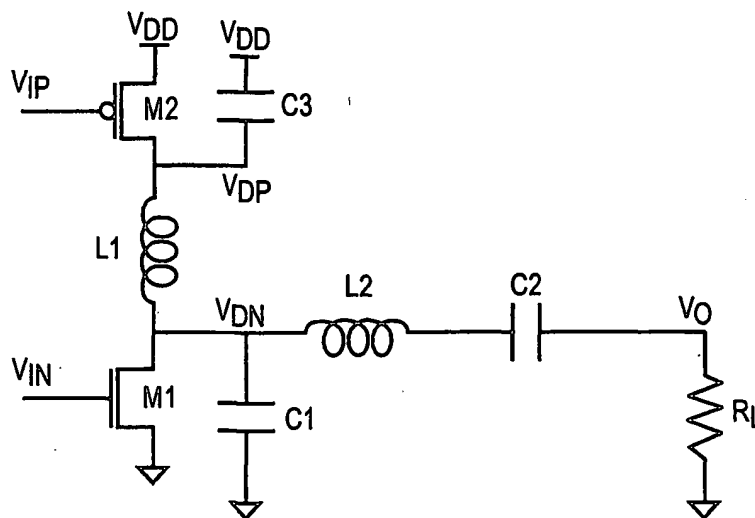


FIG. 4

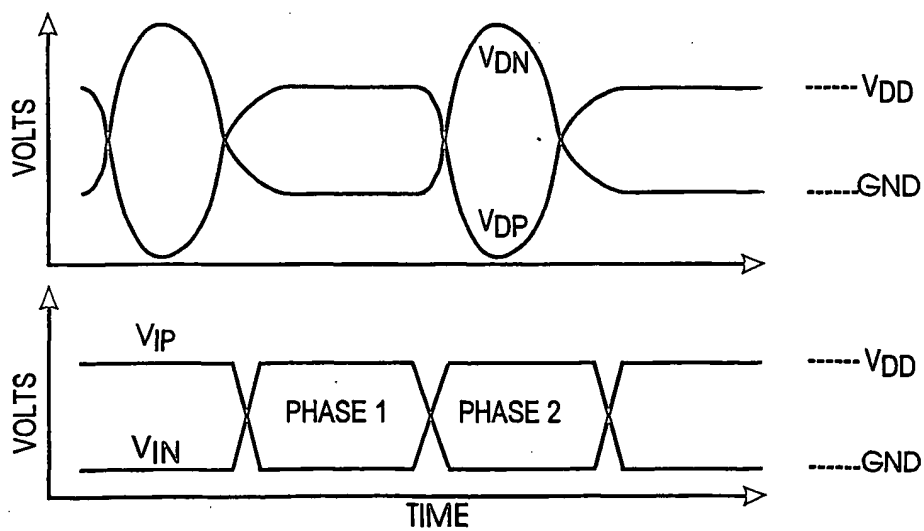


FIG. 5

3/14

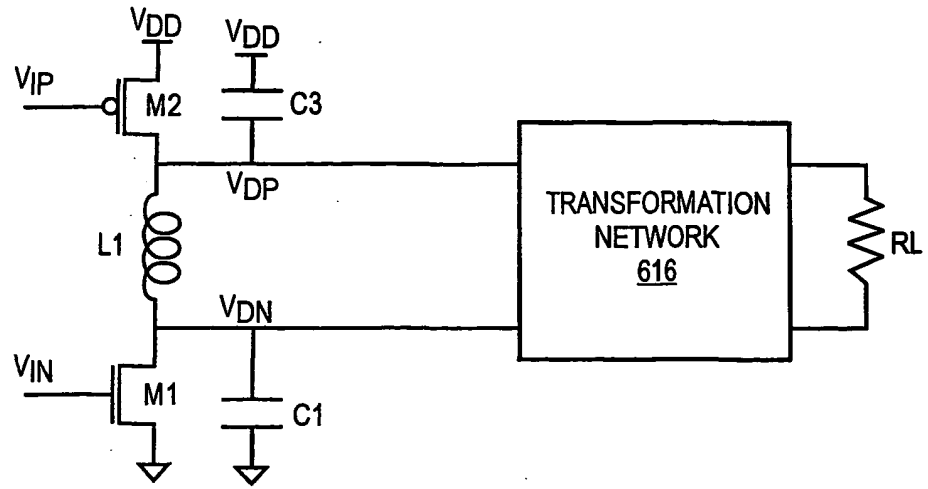


FIG. 6

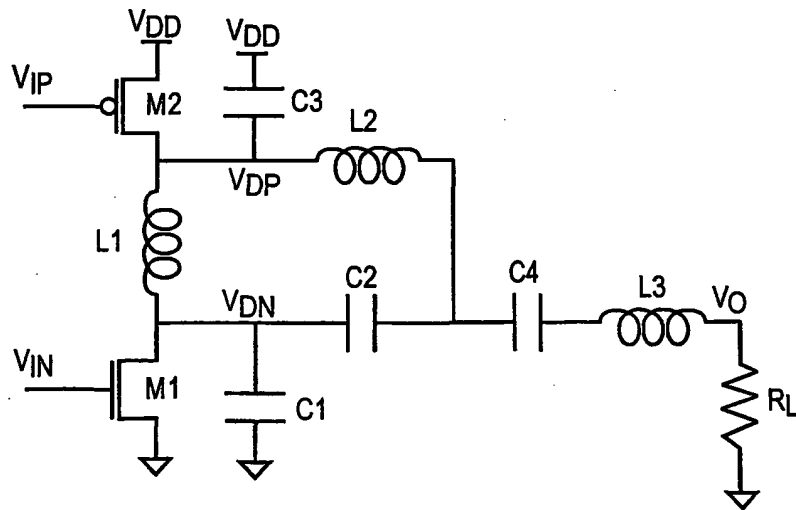


FIG. 7

4/14

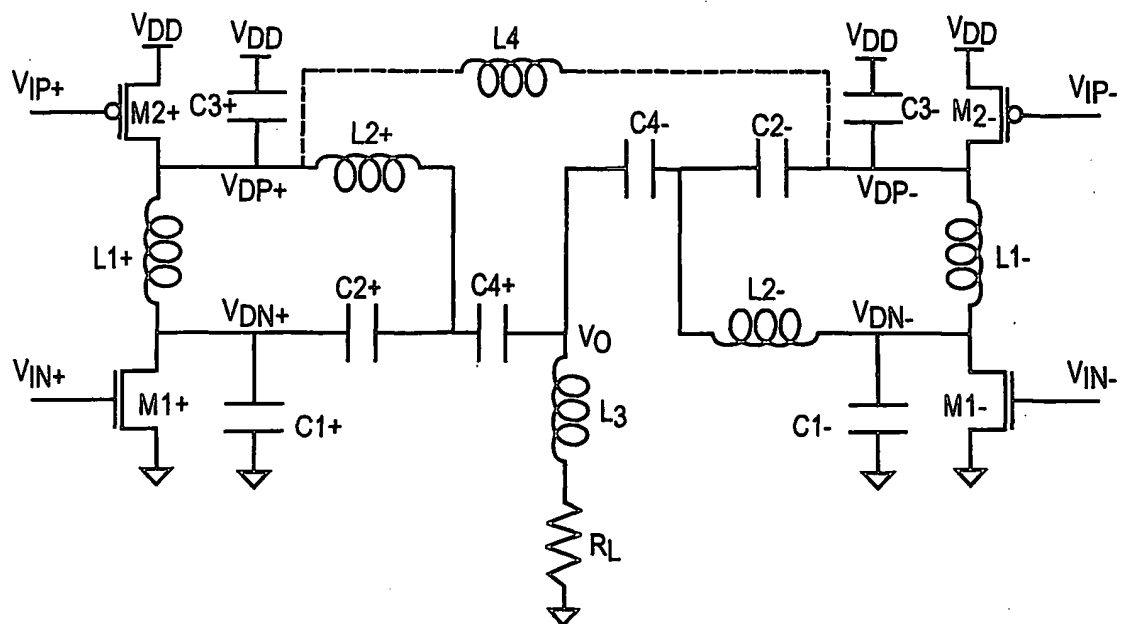


FIG. 8

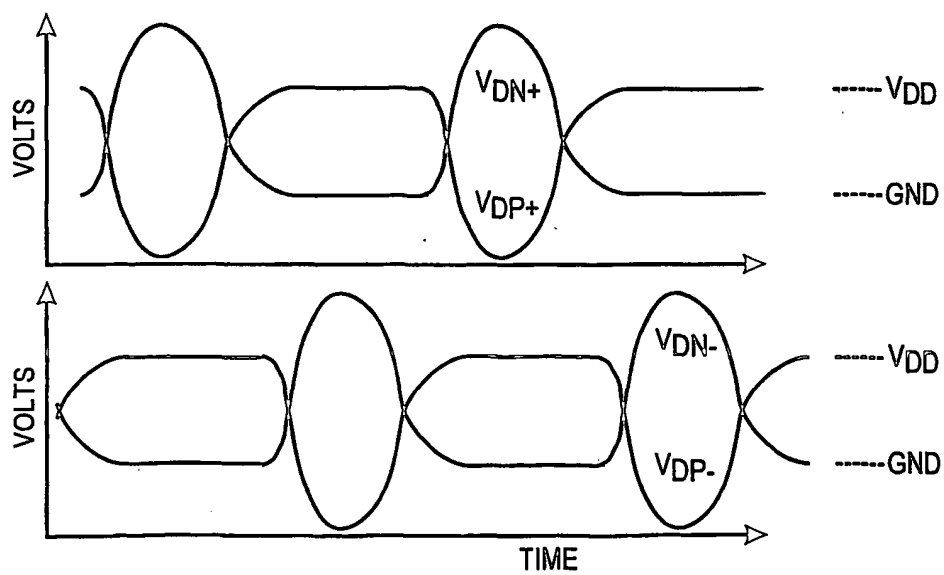


FIG. 9

5/14

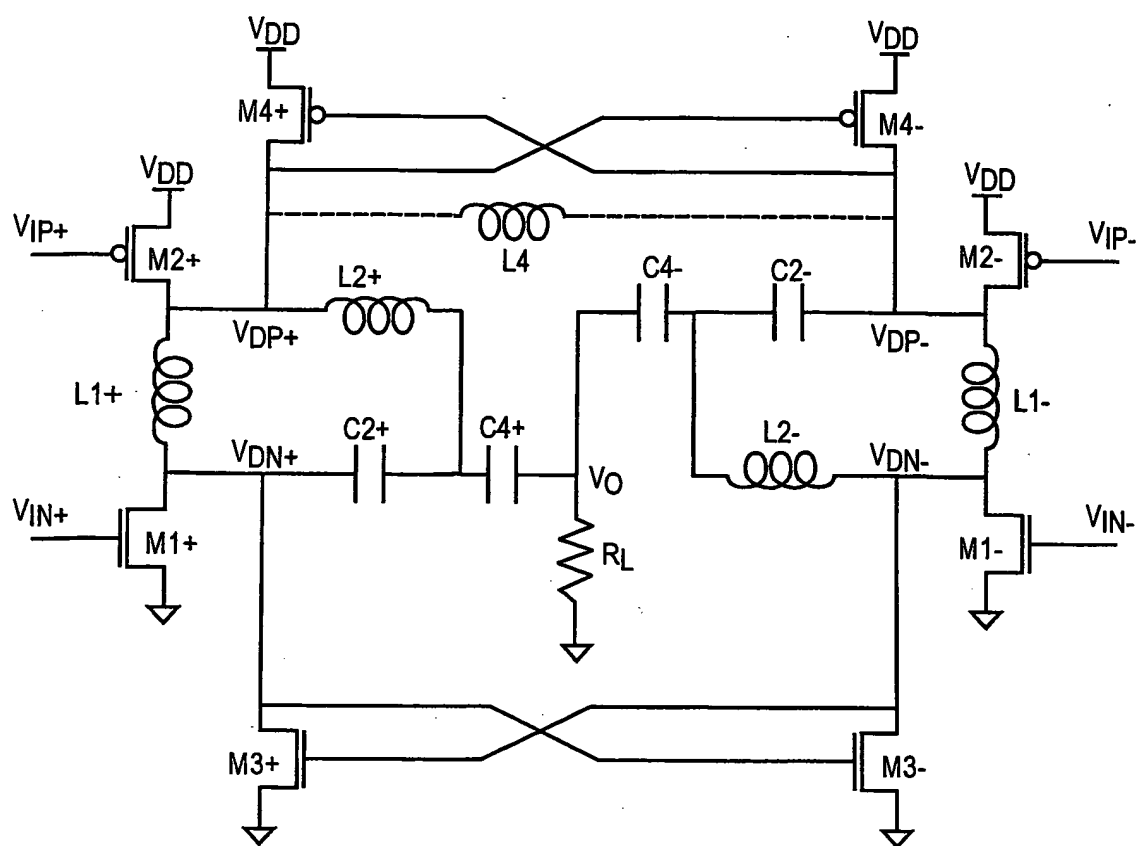


FIG. 10

7/14

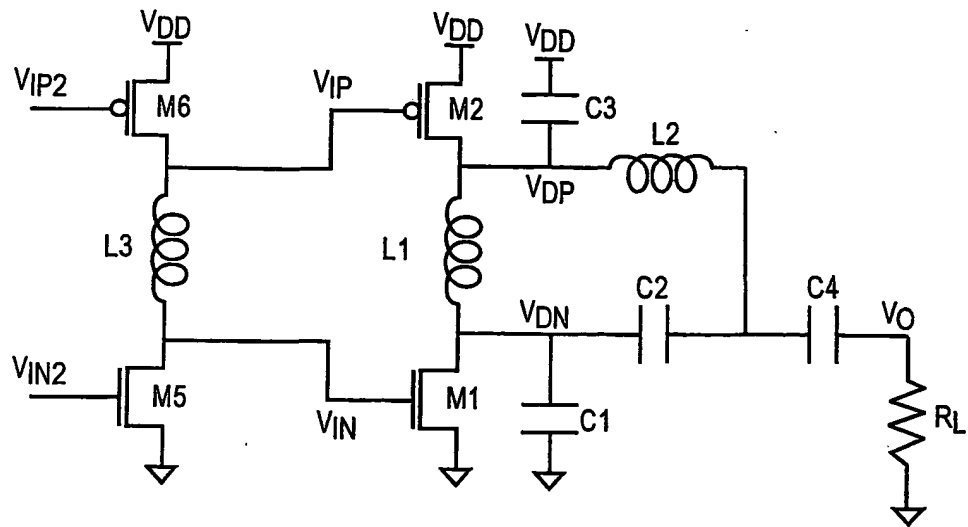


FIG. 12

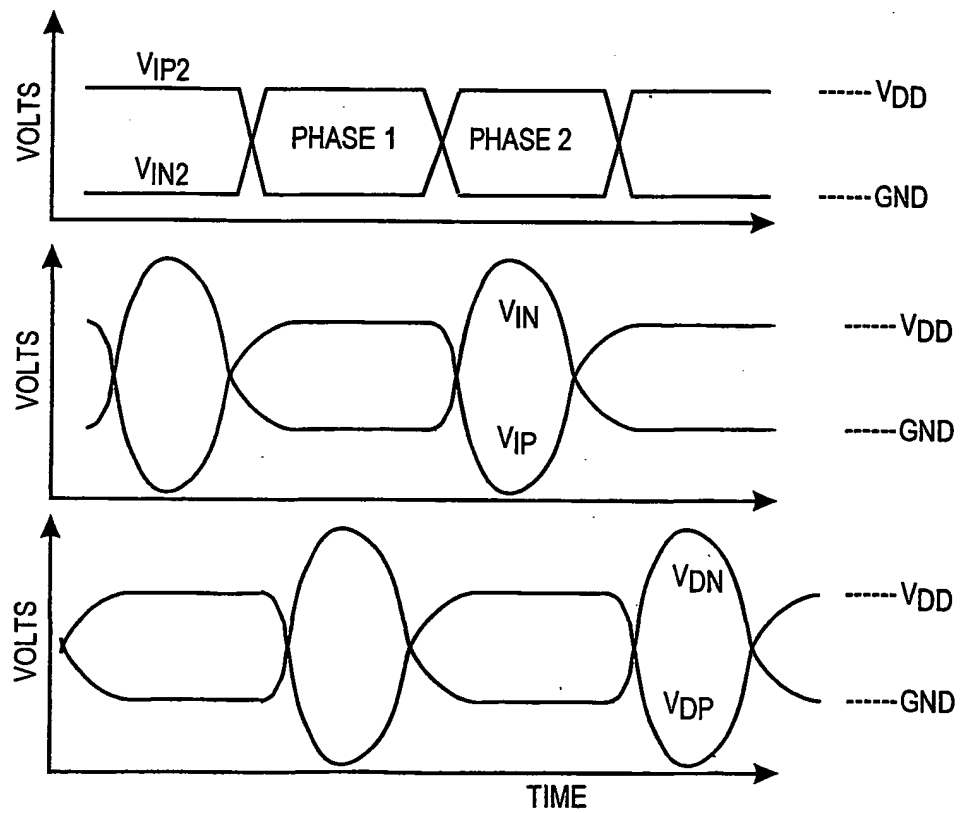


FIG. 13

8/14

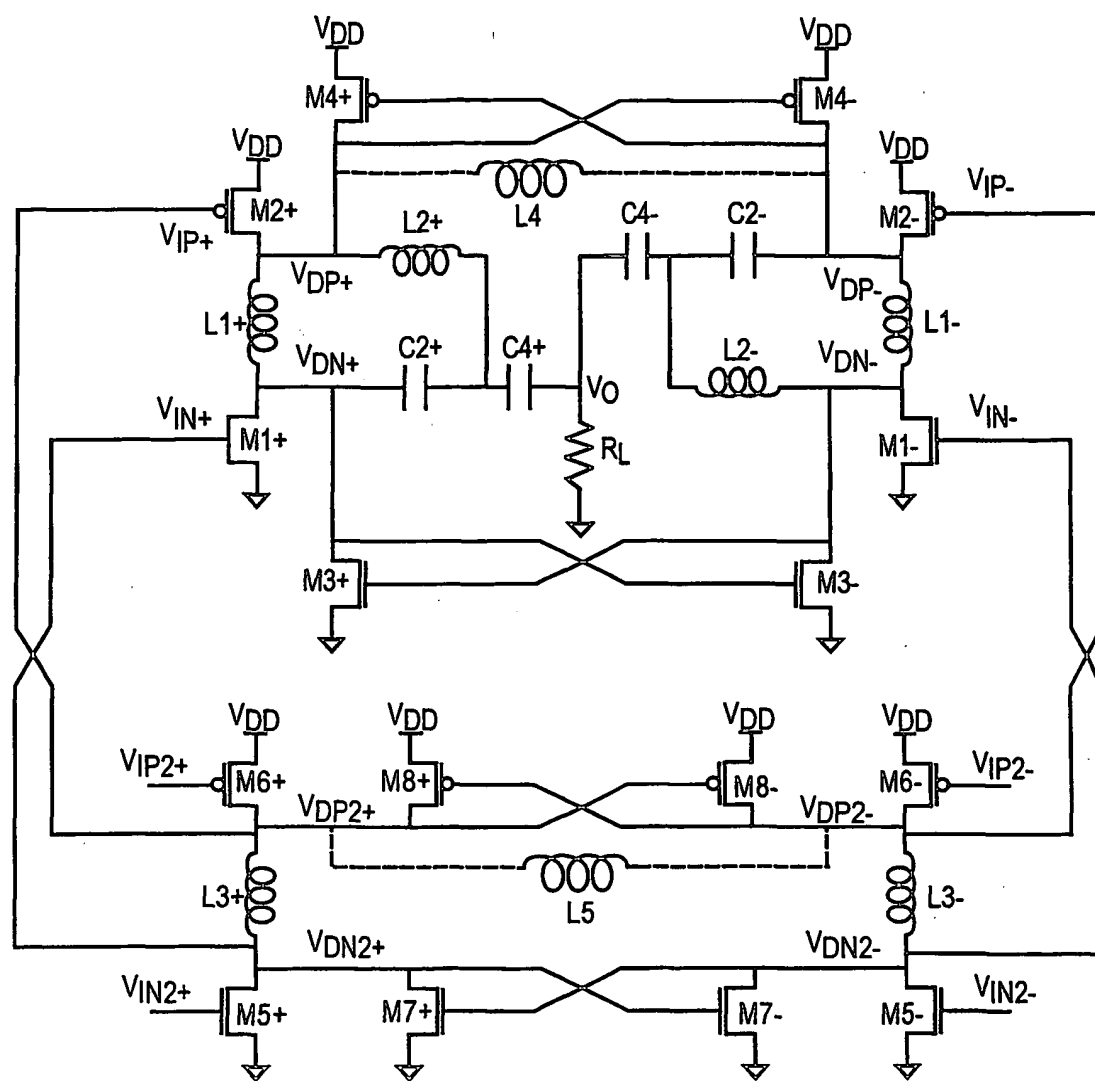


FIG. 14

9/14

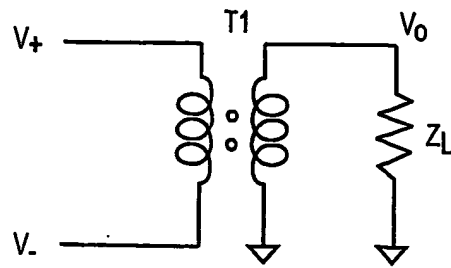


FIG. 15 (PRIOR ART)

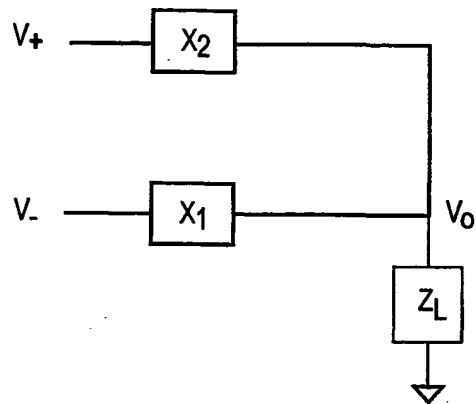


FIG. 16

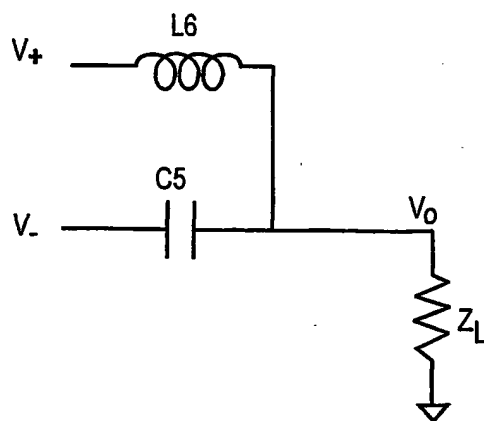


FIG. 17

10/14

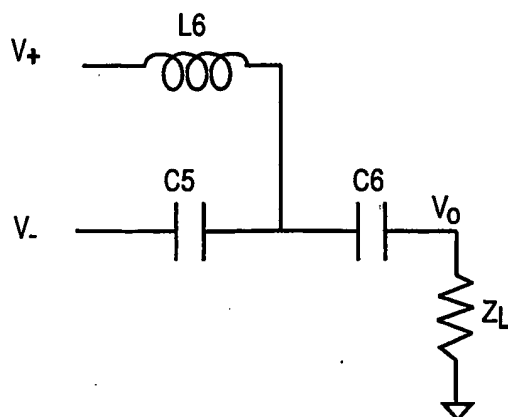


FIG. 18

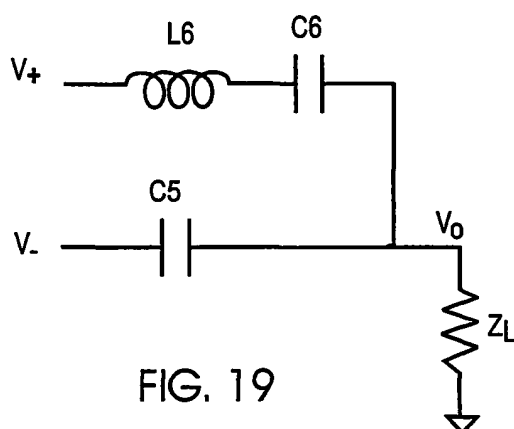


FIG. 19

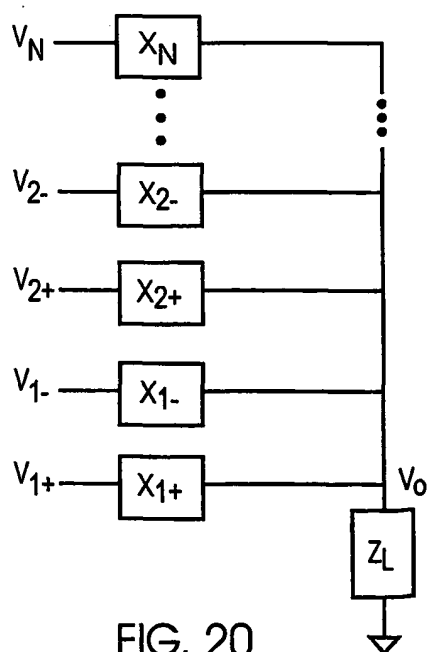


FIG. 20

11/14

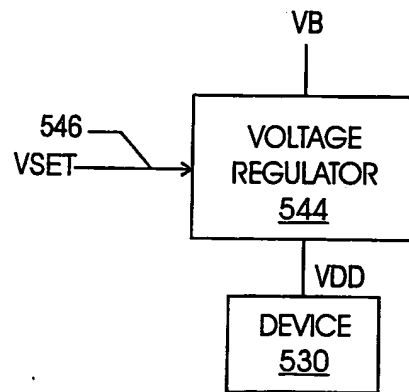


FIG. 21

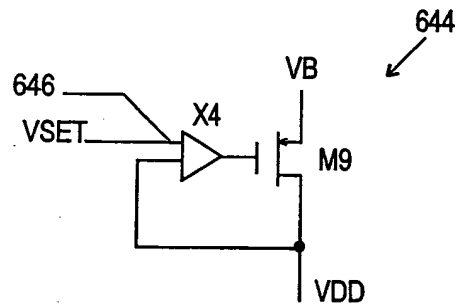


FIG. 22

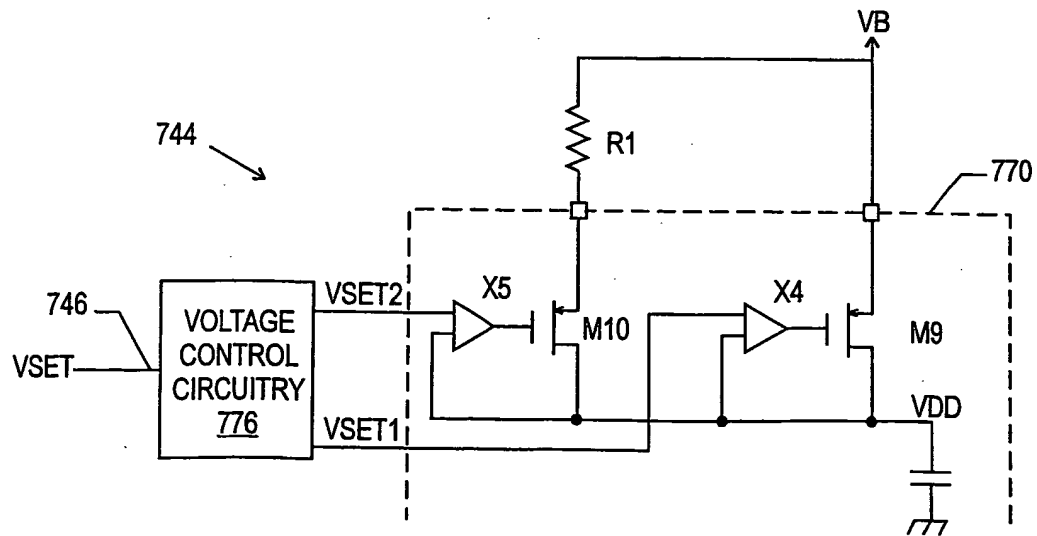


FIG. 23

12/14

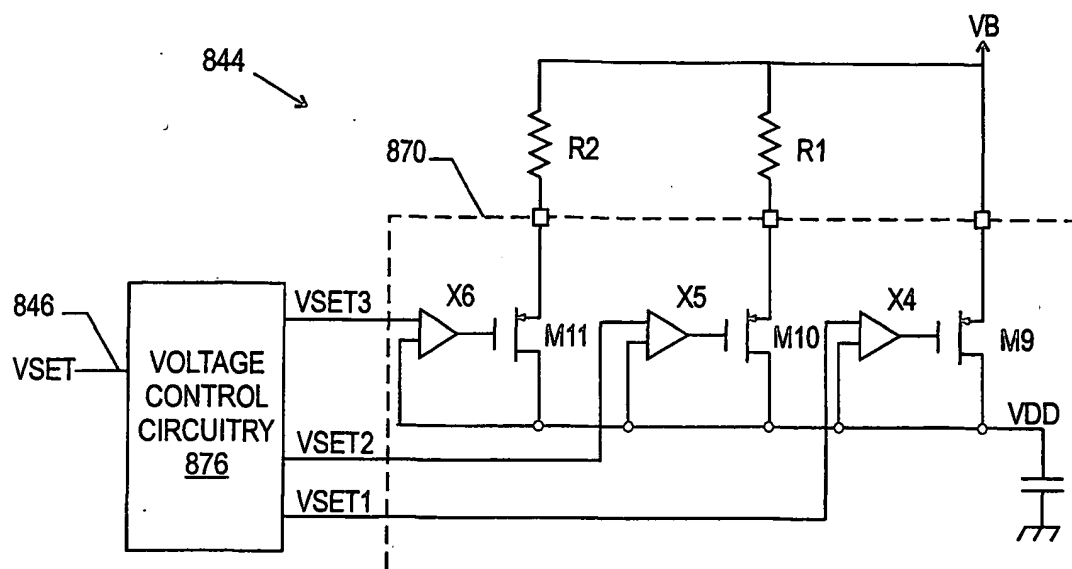


FIG. 24

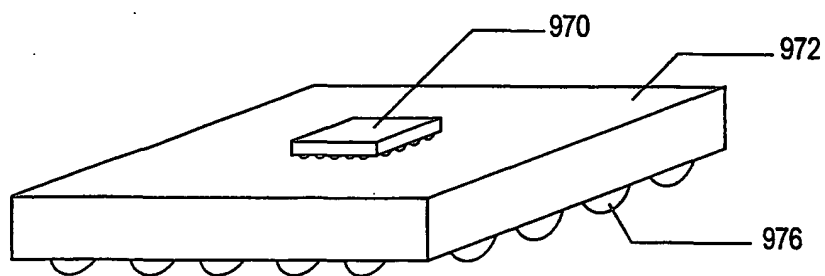


FIG. 25

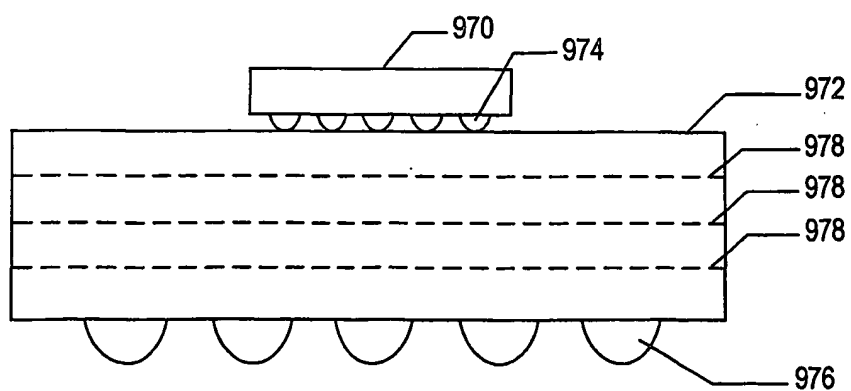


FIG. 26

13/14

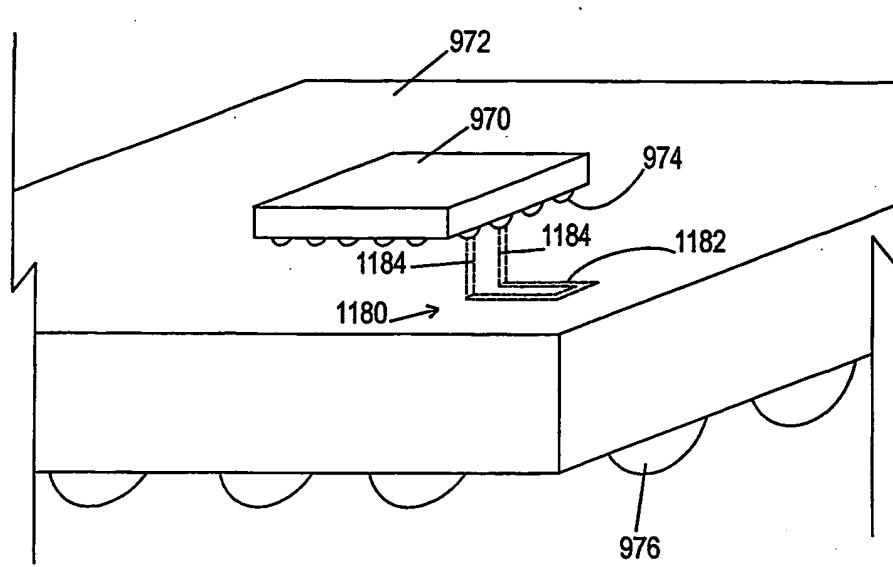


FIG. 27

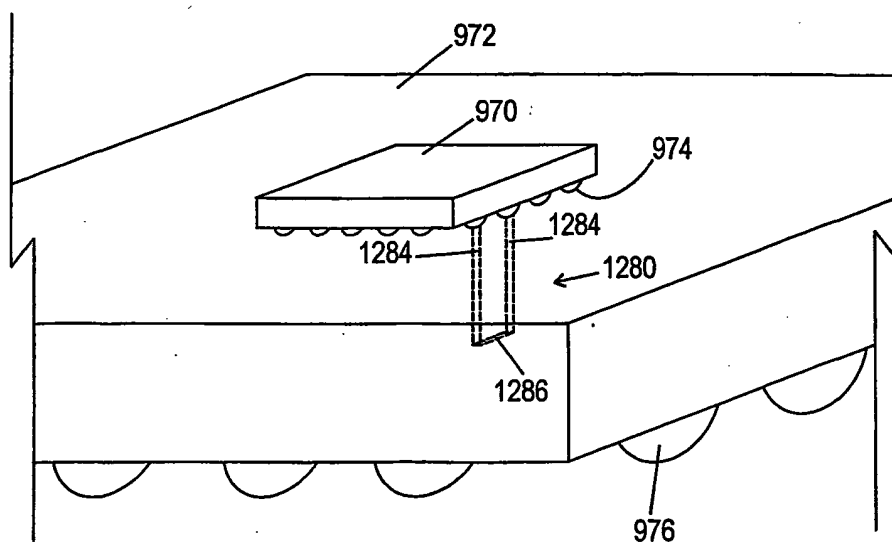


FIG. 28

14/14

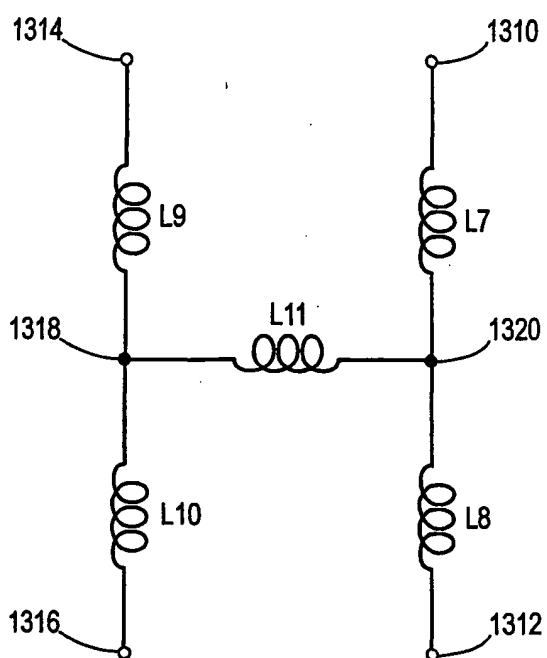


FIG. 29

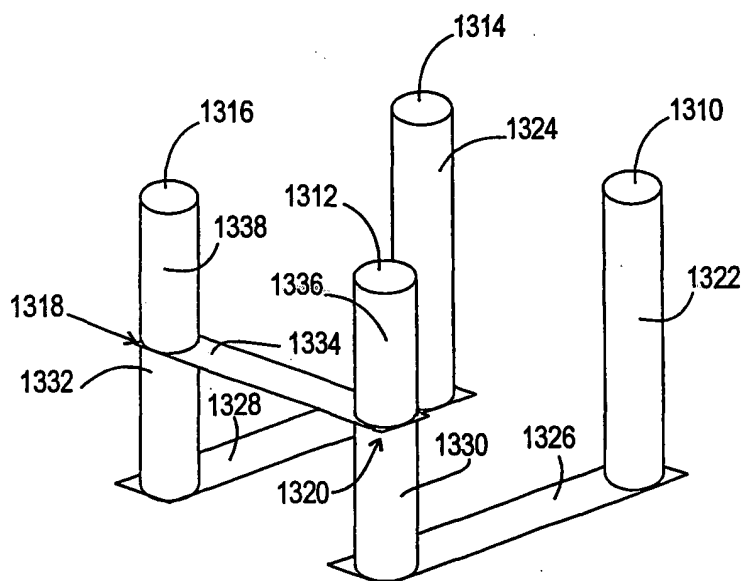


FIG. 30

